

DETAILED ACTION

Drawings

1. Figure 11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Variable Attenuator with Small Manufacturing Variation.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Koen (US 5,880,618).

In regard to Claim 1:

A variable attenuator comprising: a first signal input terminal (Figure 2: V_{inn}); a first signal output terminal (Figure 2: V_{outt}); a first control terminal receiving a control voltage (Figure 2: V_{gc}); an analog/digital converter (Figure 2: 21-1, 21-2... 21-9, 21-10) converting the control voltage to M (Figure 2: V₁, V₂, V₃, V₄... V₁₀) (M is a positive integer of 2 or more) control signals (Figure 2: 22-1, 22-2.....22-9, 22-10); and N (N is a positive integer satisfying $N \geq M$) variable impedance elements which are connected in parallel and/or in series between the first signal input terminal and the first signal output terminal (Figure 2: 20-1, 20-2...20-9, 20-10), each impedance of which being varied by either one of the control signals (Column 2: lines 62-65).

In regard to Claim 2:

The variable attenuator according to claim 1, wherein the N variable impedance elements have the same configuration and are connected in parallel between the first signal input terminal and the first signal output terminal (Column 2: lines 60-65).

In regard to Claim 3:

The variable attenuator according to claim 1, wherein the control signals are binary digital signals (Column 4: lines 34-36) having a first value and a second value, and the analog/digital converter outputs K (Figure 2: 22-1, ... 22-10)) (K is an integer satisfying $0 \leq K \leq M$) control signals having the first value and (M-K) control signals having the second value, a number of K being almost in proportion to a level of the control voltage, and N (Figure

Art Unit: 4125

2: 20-1,...20-10) and M (Figure 2: V1, ... V10) are the same value, and the N variable impedance elements (Figure 2: 20-1, ... 20-10) have the same configuration and are connected in parallel (Figure 3) between the first signal input terminal (Figure 2: Vinn) and the first signal output terminal (Figure 2: Voutt) and switched to have either one of two impedance values by the respective control signals (Column 2: lines 62-65).

In regard to Claim 7:

The variable attenuator according to claim 1, further comprising a third signal input terminal (Figure 2A: Vref) and a third signal output terminal (Figure 2A: VT1, VT2 ... VT10), wherein each variable impedance element (Figure 3: 26A) further comprises a second circuit (Figure 3: 8A) which is the same circuit as a first circuit connected between the first signal input terminal (Figure 3: Vinn) and the first signal output terminal (Figure 3: Voutt) in parallel or in series, and impedance of which is varied by the same control signal (Figure 3: V1, V2, V3 ... V10), and the second circuits (Figure 3: 8A) of the N variable impedance elements (Figure 3: 20-1, 20-2 ... 20-10) are connected in parallel or in series between the third signal input terminal (Figure 2A: Vref) and the third signal output terminal (Figure 2A: VT1, VT2 ... VT10).

In regard to Claim 8:

The variable attenuator according to claim 7, wherein the variable impedance element comprises: a second signal input terminal (Figure 3: Vinn⁺); a second signal output terminal (Figure 3: Voutt⁺); a fourth signal input terminal (Figure 3: Vinn⁻); a fourth signal output terminal (figure 3: Voutt⁻); a second control terminal receiving the control signal (Figure 3: Vcm); a constant voltage terminal (Figure 3: Vref2); a first series connector having first and second passive elements which are connected in series and inserted between the second signal

Art Unit: 4125

input terminal and the second signal output terminal (Figure 3: Rin1, also see Figure 2A where Rin1 is the plurality of resistors (61)); a second series connector having third and fourth passive elements which are connected in series and inserted between the fourth signal input terminal and the fourth signal output terminal (Figure 3: Rin2, also see Figure 2A where Rin2 is the plurality of resistors (61)); a first MOS transistor which has a drain connected to a connecting point between the first and second passive elements (Figure 3: 29-1), a source connected to the constant voltage terminal directly or through a fifth passive element (Figure 3: 29-1 and Vcm) and a gate receiving the control signal (Figure 3: 29-1 and V1); and a second MOS transistor which has a drain connected to a connecting point between the third and fourth passive elements (Figure 3: 47-1), a source connected to the constant voltage terminal directly or through the fifth passive element (Figure 3: 47-1 and Vcm), or through a sixth passive element having the same impedance as that of the fifth passive element and a gate receiving the control signal (Figure 3: 47-1 and V1).

In regard to Claim 9:

The variable attenuator according to claim 8, wherein the first, second, third, and fourth passive elements are resistors, or those passive element and the fifth passive element are resistors, or those passive elements and the fifth and sixth passive elements are resistors (Figure 2A).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 4125

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koen (US 5,880,618), in view of Takahashi (US 6,300,814).

In regard to Claim 4:

All of the claim limitations are taught with respect to Claims 1 and 3 above, except for herein the variable impedance element comprises: a second signal input terminal; a second signal output terminal; a second control terminal receiving a control signal; a constant voltage terminal; a series connector having two resistors which are connected in series and have almost the same impedance, and being inserted between the second signal input terminal and the second signal output terminal; and a switching element which is inserted between a connecting point of the two resistors and the constant voltage terminal and is turned on or off by the control signal.

Takahashi (814) teaches wherein the variable impedance element comprises: a second signal input terminal (Figure 1: 1); a second signal output terminal (Figure 1: 2); a second control terminal receiving a control signal (Figure 1: 3); a constant voltage terminal (Figure 1: 4); a series connector having two resistors which are connected in series and have almost the same impedance, and being inserted between the second signal input terminal and the second signal

Art Unit: 4125

output terminal (Figure 1: 5, 6); and a switching element which is inserted between a connecting point of the two resistors and the constant voltage terminal and is turned on or off by the control signal (Figure 1: 11).

Therefore it would have been obvious to one skilled in the art at the time of the invention to use the variable impedance element in order to decrease the attenuation error over the broad band (Column 5: lines 17-18).

In regard to Claim 5:

All of the claim limitations are taught with respect to Claim 1 above, except for the variable impedance element comprises: a second signal input terminal; a second signal output terminal; a second control terminal receiving a control signal; a constant voltage terminal; a series connector having first and second passive elements connected in series, and being inserted between the second signal input terminal and the second signal output terminal ; and a first MOS transistor which has a drain connected to a connecting point between the first and second passive elements, a source connected to the constant voltage terminal directly or through a resistor, and a gate receiving the control signal.

Takahashi (814) teaches the variable impedance element comprises: a second signal input terminal (Figure 1: 1); a second signal output terminal (Figure 1: 2); a second control terminal receiving a control signal (Figure 1: 3); a constant voltage terminal (Figure 1: 4); a series connector having first and second passive elements connected in series, and being inserted between the second signal input terminal and the second signal output terminal (Figure 1: 5, 6); and a first MOS transistor which has a drain connected to a connecting point between the first

and second passive elements, a source connected to the constant voltage terminal directly or through a resistor, and a gate receiving the control signal (Figure 1: 11).

Therefore it would have been obvious to one skilled in the art at the time of the invention to use the variable impedance element in order to decrease the attenuation error over the broad band (Column 5: lines 17-18).

In regard to Claim 6:

All of the claim limitations are taught with respect to Claims 1 and 5 above, except for the first and second passive elements are resistors.

Takahashi (814) teaches the first and second passive elements are resistors (Figure 1: 5, 6).

Therefore it would have been obvious to one skilled in the art at the time of the invention to use the variable impedance element in order to decrease the attenuation error over the broad band (Column 5: lines 17-18).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Uittenbogaard (US 7,268,606), Ehlers (US 5,666,089), and Staudinger et al. (US 5,345,123) all respectively disclose variable attenuation circuits)

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN W. POOS whose telephone number is (571)270-5077.

The examiner can normally be reached on M-F (alternating Fridays off), E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. W. P./
Examiner, Art Unit 4125

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125